IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 19, and 49 in accordance with the following:

1. (CURRENTLY AMENDED) A component-embedded board fabrication method for fabricating a component-embedded board with electronic components embedded within a wiring board, comprising:

detecting, before said board is covered with a first insulating layer, an actual position of a first electronic component formed on a surface of said board;

calculating a displacement between a design position of said first electronic component and the actual position of said first electronic component on the surface of said board, and holding said displacement as first displacement data;

determining whether the first displacement data represents a displacement that exceeds a predetermined maximum value at which the board is rendered defective;

if the represented displacement does not exceed the predetermined maximum value, correcting, based on said first displacement data, design data to be used for processing said board, ~~after~~covering said board ~~is covered~~ with said first insulating layer to form a wiring pattern connected to said first electrical component, and forming via holes in the first insulating layer in accordance with the corrected design data; and

if the represented displacement does exceed the predetermined maximum value, performing no corrections to the design data.

2. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 1, further comprising applying, based on said design data corrected in said correcting, a maskless exposure to said board covered with said first insulating layer.

3. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 1, further comprising a first direct patterning step for forming, based on said design data corrected in said first correction step, a wiring pattern by inkjetting on said board covered with said first insulating layer.

4. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 1, further comprising forming, based on said design data corrected in said correcting, a via hole in said board covered with said first insulating layer.

5. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 1, further comprising:

detecting, before said board is covered with a second insulating layer, the actual position of a second electronic component formed on a surface of said first insulating layer in which said first electronic component is already embedded;

calculating a displacement between the design position of said second electronic component and the actual position of said second electronic component on the surface of said first insulating layer, and holding said displacement as second displacement data; and

correcting, based on said second displacement data, design data to be used for processing said board after said board is covered with said second insulating layer.

6. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 1, further comprising:

capturing, before said board is covered with a second insulating layer, an image of a surface of said first insulating layer on which a second electronic component is formed and in which said first electronic component is already embedded;

calculating a displacement between the design position of said second electronic component and the actual position of said second electronic component detected from second image data obtained by imaging the surface of said first insulating layer, and holding said displacement as second displacement data; and

correcting, based on said second displacement data, design data to be used for processing said board after said board is covered with said second insulating layer.

7. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 5, further comprising applying, based on said design data corrected in said correcting, based on said second displacement data, a maskless exposure to said board covered with said second insulating layer.

8. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method

as claimed in claim 6, further comprising applying, based on said design data corrected in said correcting, based on said second displacement data, a maskless exposure to said board covered with said second insulating layer.

9. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 5, further comprising a second direct patterning step for forming, based on said design data corrected in said second correction step, a wiring pattern by inkjetting on said board covered with said second insulating layer.

10. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 6, further comprising a second direct patterning step for forming, based on said design data corrected in said second correction step, a wiring pattern by inkjetting on said board covered with said second insulating layer.

11. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 5, further comprising forming, based on said design data corrected in said correcting, based on said second displacement data, a via hole in said board covered with said second insulating layer.

12. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 6, further comprising forming, based on said design data corrected in said correcting, based on said second displacement data, a via hole in said board covered with said second insulating layer.

13. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 1, wherein when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

14. (CANCELLED)

15. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method

as claimed in claim 5, wherein when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting, based on said second displacement data, corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

16. (CANCELLED)

17. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 6, wherein when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting, based on said second displacement data, corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

18. (CANCELLED)

19. (CURRENTLY AMENDED) A component-embedded board fabrication method for fabricating a component-embedded board with electronic components embedded within a wiring board, comprising:

capturing, before said board is covered with a first insulating layer, an image of a surface of said board on which a first electronic component is formed;

calculating a displacement between a design position of said first electronic component and an actual position of said first electronic component detected from first image data obtained by imaging the surface of said board, and holding said displacement as first displacement data;

determining whether the first displacement data represents a displacement that exceeds a predetermined maximum value at which the board is rendered defective;

if the represented displacement does not exceed the predetermined maximum value, correcting, based on said first displacement data, design data to be used for processing said board, ~~after~~covering said board ~~is covered~~ with said first insulating layer to form a wiring pattern connected to said first electrical component, and forming via holes in the first insulating layer in accordance with the corrected design data; and

if the represented displacement does exceed the predetermined maximum value, performing no corrections to the design data.

20. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 19, further comprising applying, based on said design data corrected in said correcting, a maskless exposure to said board covered with said first insulating layer.

21. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 19, further comprising a first direct patterning step for forming, based on said design data corrected in said first correction step, a wiring pattern by inkjetting on said board covered with said first insulating layer.

22. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 19, further comprising forming, based on said design data corrected in said correcting, a via hole in said board covered with said first insulating layer.

23. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 19, further comprising:

detecting, before said board is covered with a second insulating layer, the actual position of a second electronic component formed on a surface of said first insulating layer in which said first electronic component is already embedded;

calculating a displacement between the design position of said second electronic component and the actual position of said second electronic component on the surface of said first insulating layer, and holding said displacement as second displacement data; and

correcting, based on said second displacement data, design data to be used for processing said board after said board is covered with said second insulating layer.

24. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 19, further comprising:

capturing, before said board is covered with a second insulating layer, an image of a surface of said first insulating layer on which a second electronic component is formed and in which said first electronic component is already embedded;

calculating a displacement between the design position of said second electronic component and the actual position of said second electronic component detected from second

image data obtained by imaging the surface of said first insulating layer, and holding said displacement as second displacement data; and

correcting, based on said second displacement data, design data to be used for processing said board after said board is covered with said second insulating layer.

25. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 23, further comprising applying, based on said design data corrected in said correcting, based on said second displacement data, a maskless exposure to said board covered with said second insulating layer.

26. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 24, further comprising applying, based on said design data corrected in said correcting, based on said second displacement data, a maskless exposure to said board covered with said second insulating layer.

27. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 23, further comprising a second direct patterning step for forming, based on said design data corrected in said second correction step, a wiring pattern by inkjetting on said board covered with said second insulating layer.

28. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 24, further comprising a second direct patterning step for forming, based on said design data corrected in said second correction step, a wiring pattern by inkjetting on said board covered with said second insulating layer.

29. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 23, further comprising forming, based on said design data corrected in said correcting, based on said second displacement data, a via hole in said board covered with said second insulating layer.

30. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 24, further comprising forming, based on said design data corrected in said correcting, based on said second displacement data, a via hole in said board covered with said second insulating layer.

31. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 19, wherein when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

32. (CANCELLED)

33. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 23 wherein, when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting, based on said second displacement data, corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

34. (CANCELLED)

35. (PREVIOUSLY PRESENTED) A component-embedded board fabrication method as claimed in claim 24 wherein, when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting, based on said second displacement data, corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

36-48. (CANCELLED)

49. (CURRENTLY AMENDED) An apparatus for fabricating a component-embedded board with electronic components embedded within a wiring board, comprising:

means for detecting, before said board is covered with a first insulating layer, an actual position of a first electronic component formed on a surface of said board;

means for calculating a displacement between a design position of said first electronic component and the actual position of said first electronic component on the surface of said board, and holding said displacement as first displacement data;

means for determining whether the first displacement data represents a displacement that exceeds a predetermined maximum value at which the board is rendered defective; and

means for correcting, based on said first displacement data, design data to be used for processing said board, ~~after~~covering said board ~~is covered~~ with said first insulating layer to form a wiring pattern connected to said first electrical component, and forming via holes in the first insulating layer in accordance with the corrected design data, only if the represented displacement does not exceed the predetermined maximum value.

50. (WITHDRAWN) The component-embedded board fabrication method of claim 1, wherein in said detecting, an optical reading device captures an image of the component-embedded board and detects the actual position of the first electronic component based on the image.